46. The system of claim 1, wherein the system bridge controller supports retry cycles when it is a master.

47. The method of claim 22, wherein the system bridge controller supports delayed read and retry of reads by external masters, thereby allowing higher I/O bus throughput.

48. The method of claim 22, wherein the system bridge controller supports retry cycles when it is a master.

49. (New) The system of claim 41, wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor, the MPEG video decoder, the means for displaying the video, and one or more of the plurality of peripheral devices.

REMARKS

Applicants appreciate the time and courtesy extended to applicants' attorney during the telephone interview of May 7, 2003, during which applicants' attorney presented an explanation to the Examiner as to why the claims of the present application are patentably distinguishable over the cited references. No agreement on the patentability was reached, however, and applicants' attorney agreed to file a response with a request for continuing examination (RCE).

While reviewing the Office Action and applicants' records of the case, applicants have noticed that there is no indication that the Examiner has considered references submitted with IDSs and Forms PTO/SB/08A/B mailed October 17, 2002 and December 12, 2002, respectively. Applicants submit herewith a copy of the above-referenced IDSs and Forms PTO/SB/08A/B for the Examiner's convenience.

Applicants respectfully request that the Examiner consider, if they have not been considered already, the references cited therein, copies of which have been provided to the Patent Office, enter copies of the signed and initialed Forms PTO/SB/08A/B in the application file, and return copies thereof along with the next communication from the Patent Office.

Claims 1-3, 5-39, 41-42 and 45-49 are pending in the present application, of which claims 1, 22 and 41 are independent. Claim 41 has been amended herein, and a new claim 49 has been added. Applicants respectfully request reconsideration and allowance of claims 1-3, 5-39, 41-42 and 45-48. Further, applicants respectfully request consideration on the merits and allowance of the newly added claim 49.

In the Office Action received via facsimile on March 12, 2003, the Examiner states that "[i]n response to applicant's argument that Fandrianto was not capable of being modified to incorporate the "north bridge" function, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . ."

Applicants respectfully submit, however, that applicants have not presented any argument regarding whether or not Fandrianto is capable of being modified to incorporate the "north bridge" function. Instead, applicants' understanding is that combination of Fandrianto and the background section of the present application, page 1, lines 9-15, to reject the claims of the present application is improper because there is no teaching, suggestion or motivation to integrate the "north bridge" function onto an integrated circuit chip with a system for processing video.

The Examiner has rejected claims 1-3, 5-39, 41-42 and 45-48 under U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,982,459 to Fandrianto et al. ("Fandrianto") in view of the background section of the present application, page 1, lines 9-15.

The Examiner agrees that "Fandrianto fails to specifically disclose '...a north bridge function...wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.'" However, the Examiner combines Fandrianto with page 2, lines 9-15 ("Video and graphics systems are typically used in television control electronics, such as set top boxes, integrated digital TVs, and home network computers. When conventional video and graphics system on integrated circuit chips are used with a host CPU in the television control electronics, a separate bridge controller, which is also referred to as a 'north bridge,' is typically used to couple the host CPU to peripheral devices") of the present application to reject the claims of the present application.

Applicants respectfully submit that this combination of references to reject the claims of the present application is improper because there is no teaching, suggestion or motivation to integrate the "north bridge" function onto an integrated circuit chip with a system for processing video. In fact, one of the problems with the prior art is given by applicants on page 183, line 35 through page 184, line 2 of the present application as "Use of the bridge controller increases number of chips in the system and introduces another potential source of system failure." This problem and the solution to the problem is not in the background section; rather, a solution provided by the present invention is a novel and unobvious way of reducing the number of chips and to avoid introducing another potential source of system failure.

The case law supports the conclusion that the fact that references can be combined or modified is not sufficient to establish a *prima facie* case of obviousness. For example, the Federal Circuit has held that "The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Mills*, 916 F.2d 680, 682, 16 USQP2d 1430, 1432 (Fed. Cir. 1990).

In *In re Mills*, claims were directed to an apparatus for producing an aerated cementitious composition by drawing air into the cementitious composition by driving the output pump at a capacity greater than the feed rate. The prior art reference taught that the feed means can be run at a variable speed, however the court found that this does not require that the output pump be run at the claimed speed so that air is drawn into the mixing chamber and is entrained in the ingredients during operation. According to the court, although a prior art device may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so. *In re Mills*, 916 F.2d at 682, 16 USPQ2d at 1432.

Similarly in the present instance, even if the integrated multimedia communications processor and codec of Fandrianto were capable of being modified to incorporate the "north bridge" function, there must be a suggestion or motivation in the references to do so. Applicants respectfully submit that there is no such suggestion or motivation in Fandrianto or in the cited passage of the background section. A "north bridge" and a system for processing video perform two completely different functions, and combining the two into a single integrated circuit chip would not have been obvious at the time of the present invention. Therefore, applicants respectfully submit that the rejection of claims 1-3, 5-39, 41-42 and 45-48 on obviousness grounds was not proper.

The conclusion that such combination is not obvious finds a further support when considering the prior art made of record and not relied upon, which the Examiner considers pertinent to the present application. These references were cited by the Examiner on Form PTO-892 at the time of mailing the Office Action mailed July 5, 2001. These reference are U.S. Patent No. 5,640,543 to Farrell et al. ("Farrell"), U.S. Patent No. 5,790,795 to Hough ("Hough") and U.S. Patent No. 6,018,803 to Kardach ("Kardach").

For example, FIG. 1 of Farrell illustrates a bridge 34 that interfaces between CPU 38 and Hard Disk 52, CD ROM 54; FIG. 4 of Hough illustrates a system bus interface 222 that interfaces between a local processor 214 and other devices on a bus 224; and FIG. 1 of Kardach illustrates a bus bridge & memory controller 108 that interfaces between a processor 100 and other devices on a peripheral bus 110.

Since none of these references appears to teach or suggest that a "north bridge" function can be integrated with a system for processing video on an integrated circuit chip despite the advantages outlined in the present application, applicants respectfully submit that these references further support the conclusion that it was not at all obvious to integrate the "north bridge" function with a system for processing video on an integrated circuit chip at the time of the present invention.

Claim 1 recites, in a relevant portion, "[a] system on an integrated circuit chip comprising: an MPEG video decoder for processing MPEG video data . . . a system bridge controller having a north bridge function for coupling a CPU to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip." This combination is neither taught nor suggested by the background of the present application and Fandrianto, either individually or jointly together. Therefore, applicants respectfully request that the rejection of claim 1 be withdrawn and that claim 1 be allowed.

Since claims 2-3 and 5-21 depend, directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 1 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 2-3 and 5-21 be withdrawn and that they be allowed.

Claim 22 recites, in a relevant portion, "coupling the CPU to a plurality of peripheral devices via a system bridge controller having

a north bridge function on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video, and wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip." This combination is neither taught nor suggested by the background of the present application and Fandrianto, either individually or jointly together. Therefore, applicants respectfully request that the rejection of claim 22 be withdrawn and that claim 22 be allowed.

Since claims 23-39 depend, directly or indirectly, from claim 22, they incorporate all the terms and limitations of claim 22 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 23-39 be withdrawn and that they be allowed.

Claim 41 recites, in a relevant portion, "[a] system on an integrated circuit chip comprising: an MPEG Transport processor . . . an MPEG video decoder . . . means for displaying the video . . . a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices, wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip." This combination is neither taught nor suggested by the background of the present application and Fandrianto, either individually or jointly together. Therefore, applicants respectfully request that the rejection of claim 41 be withdrawn and that claim 41 be allowed.

Since claim 42 depends from claim 41, it incorporates all the terms and limitations of claim 41 in addition to other limitations, which together further patentably distinguish it from the cited references. Therefore, applicants respectfully request that the rejection of claim 42 be withdrawn and that it be allowed.

The Examiner has rejected claims 45-48 without specifically addressing the limitations contained therein. For example, claim 45 and 47 recite "the system bridge controller supports delayed read and retry of reads by external masters"; and claim 46 and 48 recite "the system bridge controller supports retry cycles when it is a master". Applicants respectfully submit that these limitations are neither taught nor suggested in the cited references.

Further, since claims 45-49 depend, directly or indirectly, from claims 1, 22 and 41, respectively, they incorporate all the terms and limitations of allowable claim 1, claim 22 or claim 41, in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 45-48 be withdrawn and that claims 45-48 be allowed. Further, applicants respectfully request that claim 49 be allowed.

In view of the foregoing remarks, Applicants respectfully request allowance of claims 1-3, 5-39, 41-42 and 45-49, and an early issuance of a patent. If there are any remaining issues that can be addressed over the telephone, the Examiner is invited to call at the telephone number indicated below.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____
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Reg. No. 43,693
626/795-9900

JEJ/sd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

41. (Twice Amended) A system on an integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying;

means for displaying the video; and

a system bridge controller having a north bridge function for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices,

[~~wherein the system bridge controller performs format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and between the CPU and one or more of the plurality of peripheral devices,~~]

wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip.